i5020-T

Flash Memory Controller

Datasheet

iCreate Technologies Corporation

Data sheet marking

iCreate uses various markings in the data sheet to designate each document phase as it relates to the product development stage.

Marking	Description
Objective Specification	The objective specification contains data for new product development.
Advance Information	The information is on products in the design phase. Your designs should not be finalized with this information.
Preliminary	This is preliminary information on new products but not yet fully characterized. The specifications in these data sheets are subject to change in any manner without notice.
No Marking	Information contained in the data sheet is on products in full production.

For more information please contact:

iCreate Technologies Corporation
No. 6, Technology Rd. V, Science-Based Industrial Park,
Hsinchu, Taiwan 30077, R.O.C.
Phone +886-3-579-0000
Fax +886-3-579-0077
e-mail **support@icreate.com.tw**

Revision: 2.05
Date: 3/2003

Flash Memory Controller

1. Introduction

1.1. General description

iCreate's i5020-T is a single-chip flash memory controller IC which can control flash memories as solid state disk, and is used to build low-cost but high-performance ATA based flash memory PC Cards / CompactFlash Cards. It's in compliant with CompactFlash, PCMCIA, and ATA standards.

This controller IC has embedded flash program memory which enables firmware to be easily upgraded via specific programmer. It provides separated power supply voltage for host and flash interface to meet CompactFlash and flash memory interface requirements. An on-chip Error Correction Code (ECC) function and a wear-leveling algorithm are also implemented.

With dual-bank connection to the flash memory, the controller IC furnishes excellent performance in data transfer. It also allows direct connection of up to sixteen 1G bit flash memory chips or eight 2G bit chips for a total of 2G Byte capacity.

i5020-T is designed using 0.35-μm CMOS process, housed in 100-pin TQFP package

1.2. Features

- ✧ Embedded flash program memory for easy firmware upgrade.
- ✧ Separated power supply voltage for host and flash interface
- ✧ On-chip power-on-reset lowers entire system cost and simplifies card manufacturing.
- ✧ In Compliant with CompactFlash, PCMCIA, and ATA standards.
- ✧ 8-bit /16-bit host data transfer.
- ✧ Transfer rate up to 16.6MB/s in PIO mode 4.
- ✧ Support CFC write-protect.
- ✧ On-the-fly ECC to detect and correct errors automatically.
- ✧ Wear-leveling mechanism for memory-write maximizes data endurance.
- ✧ Support Samsung and Toshiba 64Mb to 2Gb NAND type flash chips, and will support even larger flash chips by firmware upgrade.
- ✧ Connect up to sixteen 1Gb flash chips or eight 2Gb chips for a total of 2GB capacity.

Note:
1. Support to Hitachi AND type flash memories will be available later.
2. On-chip oscillator will be available later.

1.3. Block diagram

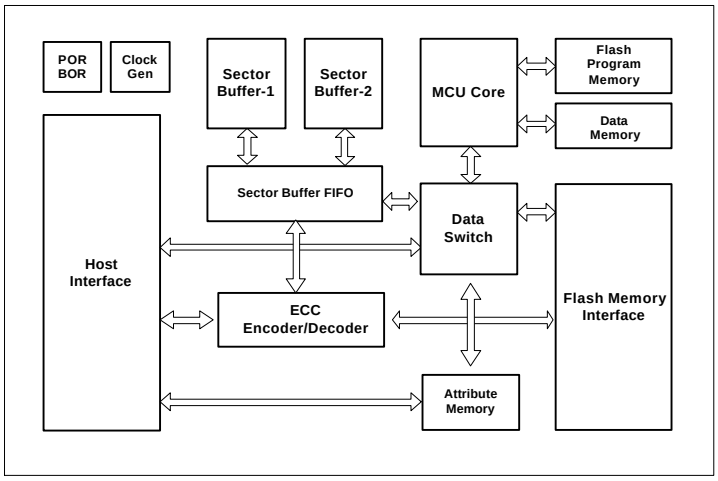


Figure 1. i5020-T block diagram

1.4. Applications

- ✧ CompactFlash card
- ✧ IDE flash disk module/chip
- ✧ PCMCIA flash card

2. Pin configuration and definition

2.1. Pin configuration

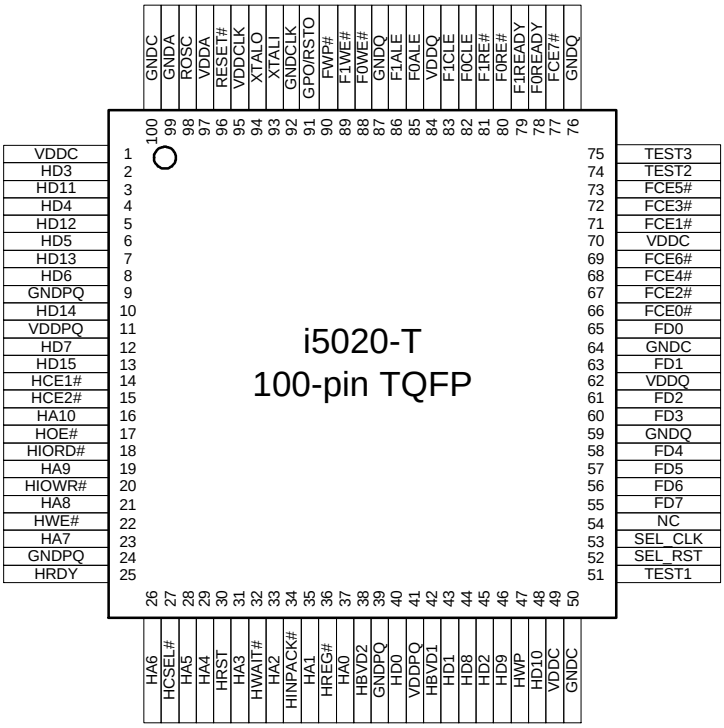


Figure 2. Pin configuration

2.2. Pin definition

2.2.1. Host interface

Pin Name	Pin No.	Signal Definition	Type	Description
HA0 ~ HA10	16, 19, 21, 23, 26, 28, 29, 31, 33, 35, 37	HA0 ~ HA10 (PC Card Memory Mode)	I	These address lines along with the REG# signal are used to select the following: The I/O port address registers within the CompactFlash Storage Card or CF+ Card, the memory mapped port address registers within the CompactFlash Storage Card or CF+ Card, a byte in the card's information structure and its configuration control and status registers.
		HA0 ~ HA10 (PC Card I/O Mode)		This signal is the same as the PC Card Memory Mode signal.
		HA0 ~ HA2 (True IDE Mode)		In True IDE Mode only HA0 ~ HA2 are used to select the one of eight registers in the Task File, the remaining address lines should be grounded by the host.

Pin Name	Pin No.	Signal Definition	Type	Description
HBVD1	42	BVD1 (PC Card Memory Mode) STSCHG# (PC Card I/O Mode) PDIAG# (True IDE Mode)	I/O	This signal is asserted high as BVD1 is not supported. This signal is asserted low to alert the host to changes in the RDY/BSY# and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Config and Status Register. In the True IDE Mode, this input/output is the Pass Diagnostic signal in the Master/Slave handshake protocol.
HBVD2	38	BVD2 (PC Card Memory Mode) SPKR# (PC Card I/O Mode) DASP# (True IDE Mode)	I/O	This signal is asserted high as BVD2 is not supported. This line is the Binary Audio output from the card. If the Card does not support the Binary Audio function, this line should be held negated. In the True IDE Mode, this input/output is the Disk Active/Slave Present signal in the Master/Slave handshake protocol.
HCE1#, HCE2#	14, 15	CE1#, CE2# (PC Card Memory Mode) Card Enable CE1#, CE2# (PC Card I/O Mode) Card Enable CS0#, CS1# (True IDE Mode)	I	These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. CE2# always accesses the odd byte of the word. CE1# accesses the even byte or the Odd byte of the word depending on HA0 and CE2#. A multiplexing scheme based on HA0, CE1#, CE2# allows 8 bit hosts to access all data on HD0~HD7. This signal is the same as the PC Card Memory Mode signal. In the True IDE Mode CS0 is the chip select for the task file registers while CS2 is used to select the Alternate Status Register and the Device Control Register.
HCSEL#	27	CSEL# (PC Card Memory Mode) CSEL# (PC Card I/O Mode) CSEL# (True IDE Mode)	I	This signal is not used in this mode. This signal is not used in this mode. This internally pulled up signal is used to configure this device as a Master or a Slave when configured in the True IDE Mode. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave.

Pin Name	Pin No.	Signal Definition	Type	Description
HD0 ~ HD15	2, 3, 4, 5, 6, 7, 8, 10, 12, 13, 40, 43, 44, 45, 46, 48	HD0 ~ HD15 (PC Card Memory Mode) HD0 ~ HD15 (PC Card I/O Mode) HD0 ~ HD15 (True IDE Mode)	I/O	These lines carry the Data, Commands and Status information between the host and the controller. HD0 is the LSB of the Even Byte of the Word. HD8 is the LSB of the Odd Byte of the Word. This signal is the same as the PC Card Memory Mode signal. In True IDE Mode, all Task File operations occur in byte mode on the low order bus HD0 ~ HD7 while all data transfers are 16 bit using HD0 ~ HD15.
HINPACK#	34	INPACK# (PC Card Memory Mode) INPACK# (PC Card I/O Mode) INPACK# (True IDE Mode)	O	This signal is not used in this mode. The Input Acknowledge signal is asserted by the CompactFlash Storage Card or CF+ Card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the CompactFlash Storage Card or CF+ Card and the CPU. In True IDE Mode this output signal is not used and should not be connected at the host.
HIORD#	18	IORD# (PC Card Memory Mode) IORD# (PC Card I/O Mode) IORD# (True IDE Mode)	I	This signal is not used in this mode. This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the Compact-Flash Storage Card or CF+ Card when the card is configured to use the I/O interface. In True IDE Mode, this signal has the same function as in PC Card I/O Mode.
HIOWR#	20	IOWR# (PC Card Memory Mode) IOWR# (PC Card I/O Mode) IOWR# (True IDE Mode)	I	This signal is not used in this mode. The I/O Write strobe pulse is use to clock I/O data on the Card Data bus into the CompactFlash Storage Card or CF+ Card controller registers when the CompactFlash Storage Card or CF+ Card is configured to use the I/O interface. In True IDE Mode, this signal has the same function as in PC Card I/O Mode.

Pin Name	Pin No.	Signal Definition	Type	Description
HOE#	17	OE# (PC Card Memory Mode) OE# (PC Card I/O Mode) ATASEL# (True IDE Mode)	I	This is an Output Enable strobe generated by the host interface. It is used to read data from the CompactFlash Storage Card or CF+ Card in Memory Mode and to read the CIS and configuration registers. In PC Card I/O Mode, this signal is used to read the CIS and configuration registers. To enable True IDE Mode, this input should be grounded by the host.
HRDY	25	RDY/BSY# (PC Card Memory Mode) IREQ# (PC Card I/O Mode) INTRQ (True IDE Mode)	O	In memory mode, this signal is set to high when the CompactFlash Storage Card or CF+ Card is ready to accept a new data transfer and held low when the card is busy. The Host memory card socket must provide a pull-up resistor. At power up and at Reset, the RDY/BSY# signal is held low (busy) until the CompactFlash Storage Card or CF+ Card has completed its power up or reset function. No access of any type should be made to the CompactFlash Storage Card or CF+ Card during this time. The RDY/ BSY# signal is held high (disabled from being busy) whenever the following condition is true: The Compact-Flash Storage Card or CF+ Card has been powered up with +RESET continuously disconnected or asserted. I/O Operation – After the CompactFlash Storage Card or CF+ Card has been configured for I/O operation, this signal is used as Interrupt Request#. This line is strobe low to generate a pulse mode interrupt or held low for a level mode interrupt. In True IDE Mode signal is the active high Interrupt Request to the host.
HREG#	36	REG# (PC Card Memory Mode) Attribute Memory Select REG# (PC Card I/O Mode) REG# (True IDE Mode)	I	This signal is used during Memory Cycles to distinguish between Common Memory and Register (Attribute) Memory accesses. High for Common Memory, Low for Attribute Memory. This signal must also be active (low) during I/O Cycles when the I/O address is on the Bus. In True IDE Mode this input signal is not used and should be connected to VCC by the host.

Pin Name	Pin No.	Signal Definition	Type	Description
HRST	30	RESET (PC Card Memory Mode) RESET (PC Card I/O Mode) RESET# (True IDE Mode)	I	When the pin is high, this signal Resets the Compact-Flash Storage Card or CF+ Card. The CompactFlash Storage Card or CF+ Card is Reset only at power up if this pin is left high or open from power-up. The CompactFlash Storage Card or CF+ Card is also Reset when the Soft Reset bit in the Card Configuration Option Register is set. This signal is the same as the PC Card Memory Mode signal. In the True IDE Mode this input pin is the active low hardware reset from the host.
HWAIT#	32	WAIT# (PC Card Memory Mode) WAIT# (PC Card I/O Mode) IORDY (True IDE Mode)	O	The WAIT# signal is driven low by the CompactFlash Storage Card or CF+ Card to signal the host to delay completion of a memory or I/O cycle that is in progress. This signal is the same as the PC Card Memory Mode signal. In True IDE Mode this output signal may be used as IORDY.
HWE#	22	WE# (PC Card Memory Mode) WE# (PC Card I/O Mode) WE# (True IDE Mode)	I	This is a signal driven by the host and used for strobing memory write data to the registers of the CompactFlash Storage Card or CF+ Card when the card is configured in the memory interface mode. It is also used for writing the configuration registers. In PC Card I/O Mode, this signal is used for writing the configuration registers. In True IDE Mode this inputs signal is not used and should be connected to VCC by the host.
HWP	47	WP (PC Card Memory Mode) Write Protect IOIS16# (PC Card I/O Mode) IOIS16# (True IDE Mode)	O	Memory Mode – The CompactFlash Storage Card or CF+ Card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence. I/O Operation – When the CompactFlash Storage Card or CF+ Card is configured for I/O Operation this pin is used for the I/O Selected# is 16 Bit Port (IOIS16#) function. A Low signal indicates that a 16 bit or odd byte only operation can be performed at the addressed port. In True IDE Mode this output signal is asserted low when this device is expecting a word data transfer cycle.

2.2.2. Flash interface

Pin Name	Pin No.	Pin Type	Description
FD0 ~ FD7	55, 56, 57, 58, 60, 61, 63, 65	I/O	Flash Data Bus 0 ~ 7. Connect to flash memory pins FD0 ~ FD7.
F0ALE F1ALE	85, 86	O	NAND Type: Flash Address Latch Enable. Connect to flash memory pin ALE. AND Type: Serial Clock. Connect to flash memory pin SC.
F0CLE F1CLE	82, 83	O	NAND Type: Flash Command Latch Enable. Connect to flash memory pin CLE AND Type: Command Data Enable. Connect to flash memory pin CDE.
F0RE# F1RE# F0WE# F1WE#	80, 81, 88, 89	O	NAND Type: Flash Read/Write Enable. Connect to flash memory pin RE/WE. AND Type: F0RE# and F1RE# are connected to Output Enable of flash.
FCE0# ~ FCE7#	66, 67, 68, 69, 71, 72, 73, 77	O	Flash Chip Enable. Connect to flash memory pin CE.
FWP#	90	O	NAND Type: Flash Write-Protect. Connect to flash memory pin WP. AND Type: Flash Reset Signal. Connect to flash memory pin Reset.
F0READY F1READY	78, 79	I	Flash Ready/BSY signal. Connect to flash memory pin Ready/Busy#.

2.2.3. System interface

Pin Name	Pin No.	Pin Type	Description
GPO/RSTO	91	O	Reset output or general purpose output for testing
SEL_CLK	53	I	Select internal or external oscillator in normal mode.
SEL_RST	52	I	Select internal or external reset in normal mode.
TEST1 TEST2 TEST3	51 74 75	I	Test pin 1 and test pin 2. These pins should be connected to GND in normal operation.
XTALO	94	O	Crystal output
XTALI	93	I	Crystal input
RESET#	96	I	Reset input if reset is provided externally.
VDDC	1, 49, 70		3.3V power for core
GNDC	50, 64, 100		Ground for core
VDDQ	62, 84		3.3V power for flash interface
GNDQ	59, 76, 87		Ground for 3.3V flash interface
VDDPQ	11, 41		Directly connected to host VDD for host interface I/O. Can be 5.0V or 3.3V.

Pin Name	Pin No.	Pin Type	Description
GNDPQ	9, 24, 39		Ground for host interface
VDDA	97		3.3V power for analog circuit
GNDA	99		Ground for analog circuit
VDDCLK	95		3.3V Power for oscillator
GNDCLK	92		Ground for oscillator

2.2.4. Pin direction, operating voltage and pull-up/pull-down

Due to the optional pull-up/pull-down of some signals in CF specification and the different definitions in different products, several pins can be pull-up or pull-down through firmware.

* The pin operating voltages are defined as: (1) HI, HO and HIO: 3.3V/5.0V. (2) AI, HV, NI, NIO, OSCI, OSCO: 3.3V.
* The pull-up/pull-down abbreviations are: (1) PD: fixed pull-down. (2) PU: fix pull-up. (3) PPD: programmable pull-down. (3) PPU1: programmable pull-up group 1. (4) PPU2: programmable pull-up group 2.

Pin #	Name	Type	Pull-up/Pull-down	Pin #	Name	Type	Pull-up/Pull-down
1	VDDC	—	—	**51**	TEST1	NI	—
2	HD3	HIO	PPD	**52**	SEL_RST	AI	—
3	HD11	HIO	PPD	**53**	SEL_CLK	AI	—
4	HD4	HIO	PPD	**54**	NC	—	—
5	HD12	HIO	PPD	**55**	FD7	NIO	PPU1
6	HD5	HIO	PPD	**56**	FD6	NIO	PPU1
7	HD13	HIO	PPD	**57**	FD5	NIO	PPU1
8	HD6	HIO	PPD	**58**	FD4	NIO	PPU1
9	GNDPQ	—	—	**59**	GNDQ	—	—
10	HD14	HIO	PPD	**60**	FD3	NIO	PPU1
11	VDDPQ	—	—	**61**	FD2	NIO	PPU1
12	HD7	HIO	PPD	**62**	VDDQ	—	—
13	HD15	HIO	PPD	**63**	FD1	NIO	PPU1
14	HCE1#	HI	PU	**64**	GNDC	—	—
15	HCE2#	HI	PU	**65**	FD0	NIO	PPU1
16	HA10	HI	PPD	**66**	FCE0#	NIO	—
17	HOE#	HI	PU	**67**	FCE2#	NIO	—
18	HIORD#	HI	PU	**68**	FCE4#	NIO	—
19	HA9	HI	PPD	**69**	FCE6#	NIO	—
20	HIOWR#	HI	PU	**70**	VDDQ	—	—
21	HA8	HI	PPD	**71**	FCE1#	NIO	—
22	HWE#	HI	PU	**72**	FCE3#	NIO	—
23	HA7	HI	PPD	**73**	FCE5#	NIO	—

Pin #	Name	Type	Pull-up/Pull-down	Pin #	Name	Type	Pull-up/Pull-down
24	GNDPQ	—	—	**74**	TEST2	NI	—
25	HRDY	HO	—	**75**	TEST3	NI	—
26	HA6	HI	PPD	**76**	GNDQ	—	—
27	HCSEL#	HI	PU	**77**	FCE7#	NIO	—
28	HA5	HI	PPD	**78**	F0READY	NI	PU
29	HA4	HI	PPD	**79**	F1READY	NI	PU
30	HRST	HI	PU	**80**	F0RE#	NIO	—
31	HA3	HI	PPD	**81**	F1RE#	NIO	—
32	HWAIT#	HO	—	**82**	F0CLE	NIO	—
33	HA2	HI	PPD	**83**	F1CLE	NIO	—
34	HINPACK#	HO	—	**84**	VDDQ	—	—
35	HA1	HI	PPD	**85**	F0ALE	NIO	—
36	HREG#	HI	PU	**86**	F1ALE	NIO	—
37	HA0	HI	PPD	**87**	GNDQ	—	—
38	HBVD2	HIO	PPU2	**88**	F0WE#	NIO	—
39	GNDPQ	—	—	**89**	F1WE#	NIO	—
40	HD0	HIO	PPD	**90**	FWP#	NIO	—
41	VDDPQ	—	—	**91**	GPO	NIO	—
42	HBVD1	HIO	PPU2	**92**	GNDCLK	—	—
43	HD1	HIO	PPD	**93**	XTALI	OSCI	—
44	HD8	HIO	PPD	**94**	XTALO	OSCO	—
45	HD2	HIO	PPD	**95**	VDDCLK	—	—
46	HD9	HIO	PPD	**96**	RESET#	AI	—
47	HWP	HO	—	**97**	VDDA	—	—
48	HD10	HIO	PPD	**98**	ROSC	AI	—
49	VDDC	—	—	**99**	GNDA	—	—
50	GNDC	—	—	**100**	GNDC	—	—

3. Typical CIS contents

The following CIS table is for reference only and can be programmed as requested.

CIS Tuple Name	Contents	Description
CISTPL_DEVICE	0x01, 0x04, 0xDF, 0x4A, 0x01, 0xFF	Device info for common memory
CISTPL_DEVICE_OC	0x1C, 0x04, 0x02, 0xD9, 0x01, 0xFF	Other conditions device information
CISTPL_JEDEC_C	0x18, 0x02, 0xDF, 0x01	JEDEC manufacturing and programming algorithms
CISTPL_MANFID	0x20, 0x04, 0x07, 0x00, 0x00, 0x00	PCMCIA manufacturers ID
CISTPL_VERS_1	0x15, 0x15, 0x04, 0x01, “iCreate”, 0, “FLASH”, 0, ”1.0”, 0, 0xFF	PCMCIA compliance level of the CIS
CISTPL_FUNCID	0x21, 0x02, 0x04, 0x01	Function identification
CISTPL_FUNCE	0x22, 0x02, 0x01, 0x01	Function extension
CISTPL_FUNCE	0x22, 0x03, 0x02, 0x0C, 0x0F	Function extension
CISTPL_CONFIG	0x1A, 0x05, 0x01, 0x03, 0x00, 0x02, 0x0F	Configuration
CISTPL_CFTABLE_ENTRY	0x1B, 0x08, 0xc0, 0x40, 0xA1, 0x01, 0x55, 0x08, 0x00, 0x20	Config. table entry
CISTPL_CFTABLE_ENTRY	0x1B, 0x06, 0x00, 0x01, 0x21, 0xB5, 0x1E, 0x4D	Config. table entry
CISTPL_CFTABLE_ENTRY	0x1B, 0x0A, 0xC1, 0x41, 0x99, 0x01, 0x55, 0x64, 0xF0, 0xFF, 0xFF, 0x20	Config. table entry
CISTPL_CFTABLE_ENTRY	0x1B, 0x06, 0x01, 0x01, 0x21, 0xB5, 0x1E, 0x4D	Config. table entry

CIS Tuple Name	Contents	Description
CISTPL_CFTABLE_ENTRY	0x1B, 0x0F, 0xC2, 0x41, 0x99, 0x01, 0x55, 0xEA, 0x61, 0xF0, 0x01, 0x07, 0xF6, 0x03, 0x01, 0xEE, 0x20	Config. table entry
CISTPL_CFTABLE_ENTRY	0x1B, 0x06, 0x02, 0x01, 0x21, 0xB5, 0x1E, 0x4D	Config. table entry
CISTPL_CFTABLE_ENTRY	0x1B, 0x0F, 0xC3, 0x41, 0x99, 0x01, 0x55, 0xEA, 0x61, 0x70, 0x01, 0x07, 0x76, 0x03, 0x01, 0xEE, 0x20	Config. table entry
CISTPL_CFTABLE_ENTRY	0x1B, 0x06, 0x03, 0x01, 0x21, 0xB5, 0x1E, 0x4D	Config. table entry
CISTPL_NO_LINK	0x14, 0x00	No link after the END tuple

4. Special functions

4.1. Power-on-reset and brown-out-reset

The internal reset control unit has power-on-reset (POR) and brown-out-reset (BOR) functions. The reset state will be kept until the system voltage is stabilized. When the system voltage drops below the threshold, reset is also initiated to halt operations to avoid unexpected results. To use internal POR, set SEL_RST to 1 and RESET# must be connected to an external RC network. To use external reset signal, set SEL_RST to 0 and RESET# becomes the reset signal input. The threshold voltage is 2.7V±200mV, and the hold time of RESET# is $0.7R_{ext1}C_{ext}$.

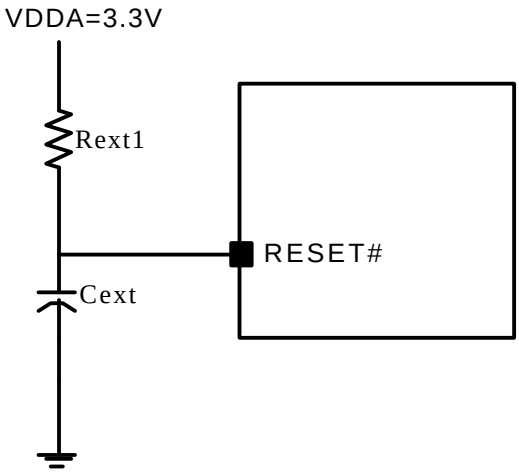


Figure 3. Connection using internal power-on-reset/brown-out-reset

4.2. Internal RC oscillator

An embedded RC oscillator can be used to reduce system cost. However, the user can still use an external clock source up to 24 MHz. When the internal oscillator is used, ROSC must be connected to GND through a resistor, as shown in the following figure. XTALI and XTALO can be floating if internal oscillator is used.

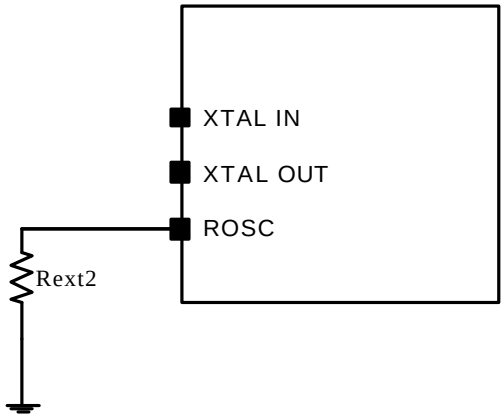


Figure 4. Connection using internal Oscillator

4.3. Flash programming through host interface

Embedded flash can be programmed even after the chip was soldered on board. For this purpose, all the signals that are required to program the embedded flash are accessible through the host interface. Since flash programming is still under normal mode, all the configurations such as internal/external reset, internal/external clock are as the normal mode. Chip will enter programming mode through special signal combinations at the host interface, which will not conflict with standard PCMCIA/ATA/CF host operation, but the programming requires a special writer. For more information, please contact distributors or iCreate sales representatives.

5. Electrical specifications

5.1. DC characteristics

5.1.1. Absolute maximum ratings

Symbol	Description	Value	Unit	Notes
V_{CC}	V_{CC} Voltage	–0.3 to +6.5	V	VDDPQ
V_{DD}	V_{DD} Voltage	-0.3 to +4.6	V	VDDC, VDDQ
V_{IN}, V_{OUT}	All input/output voltages	–0.3 to V_{CC} + 0.3	V	For host interface
V_{IN}, V_{OUT}		–0.3 to V_{DD} + 0.3	V	For other I/O except host interface
Topr	Operating temperature range	0 to +70	°C	
Tstg	Storage temperature range	–55 to +125	°C	

5.1.2. Recommended operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	V_{CC} Voltage	4.5	5	5.5	V
		3.15	3.3	3.45	V
V_{DD}	V_{DD} Voltage	3.15	3.3	3.45	V
T_{OPR}	Operating temperature	0		70	^{o}C

5.1.3. General DC characteristics

(Ta= 0 to 70 ^{o}C, V_{DD}= 3.3V ± 5%)

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{IL}	Input LOW voltage			0.8	V
V_{IH}	Input HIGH voltage		2.0		V
V_{OL}	Output LOW voltage			0.4	V
V_{OH}	Output HIGH voltage	V_{CC} = 3.3V ± 5%	2.4		V
		V_{CC} = 5.0V ± 10%	2.8 (TTL) 4.0 (CMOS)		V

5.1.4. Power-on-reset characteristics

Symbol	Parameter	Typ.	Unit
V_T(RESET)	Threshold voltage of V_{CC} to activate/de-activate reset	2.7	V
th(RESET)	Hold time of reset after V_{CC} rises above V_T	$0.7R_{ext1}C_{ext}$*	s

*: R_{ext1} and C_{ext} are defined in “Power-on-reset and brown-out-reset”.

5.2. AC characteristics

Test conditions: Ta = 0 to +70° C, VCC = 5.0 V ± 10% or VCC = 3.3 V ± 5%, VDD = 3.3 V ± 5%

5.2.1. Reset characteristics

Symbol	Parameter	Min.	Max.	Unit
tsu(RESET)	Reset high setup time for CE	100		ms
tpr	V_{CC} rising up time	0.1	100	ms
tpf	V_{CC} falling down time	3	300	ms
tw(RESET)	Reset pulse width	10		μs

5.2.2. Attribute memory read and write AC characteristics

For the definitions of parameters, please refer to CompactFlash Specification.

Symbol	Parameter	Min.	Max.	Unit
tcR	Read cycle time	250		ns
ta(A)	Address access time		250	ns
ta(CE)	Card Enable access time		250	ns
ta(OE)	Output Enable access time		125	ns
tdis(CE)	Output disable time from CE		100	ns
tdis(OE)	Output disable time from OE		100	ns
ten(CE)	Output enable time from CE	5		ns
ten(OE)	Output enable time from OE	5		ns
tv(A)	Data valid time from address change	0		ns
tsu(A)	Address setup time	30		ns
tcW	Write cycle time	250		ns
tw(WE)	Write pulse time	150		ns
trec(WE)	Write recovery time	30		ns
tsu(D-WEH)	Data setup time for WE	80		ns
th(D)	Data hold time	30		ns
trec(WE)	Write recover time	30		ns

5.2.3. Common memory read and write AC characteristics

For the definitions of parameters, please refer to CompactFlash Specification.

Symbol	Parameter	Min.	Max.	Unit
ta(OE)	Output Enable access time		125	ns
tdis(OE)	Output disable time from OE		100	ns
tsu(A)	Address setup time	30		ns
th(A)	Address hold time	20		ns

Symbol	Parameter	Min.	Max.	Unit
tsu(CE)	Card Enable setup time	0		ns
th(CE)	Card Enable hold time	20		ns
tw(WE)	Write pulse time	150		ns
tsu(D-WEH)	Data setup time for WE	80		ns
th(D)	Data hold time	30		ns
trec(WE)	Write recover time	30		ns

5.2.4. I/O access read and write AC characteristics

For the definitions of parameters, please refer to CompactFlash Specification.

Symbol	Parameter	Min.	Max.	Unit
td(IORD)	Data delay after IORD		100	ns
th(IORD)	Data hold time following IORD	0		ns
tw(IORD)	IORD pulse width	165		ns
tsuA(IORD)	Address setup time for IORD	70		ns
thA(IORD)	Address hold time from IORD	20		ns
tsuCE(IORD)	Card Enable setup time for IORD	5		ns
thCE(IORD)	Card Enable hold time from IORD	20		ns
tsuREG(IORD)	REG setup time for IORD	5		ns
thREG(IORD)	REG hold time from IORD	0		ns
tdfINP(IORD)	INPACK delay falling from IORD	0	45	ns
tdrINP(IORD)	INPACK delay rising from IORD		45	ns
tdfIO16(IORD)	IOIS16 delay falling from address		35	ns
tdrIO16(IORD)	IOIS16 delay rising from address		35	ns
tsu(IOWR)	Data setup time for IOWR	60		ns
th(IOWR)	Data hold time from IOWR	30		ns
tw(IOWR)	IOWR pulse width	165		ns
tsuA(IOWR)	Address setup time for IOWR	70		ns
thA(IOWR)	Address hold time from IOWR	20		ns
tsuCE(IOWR)	Card Enable setup time for IOWR	5		ns
thCE(IOWR)	Card Enable hold time from IOWR	20		ns
tsuREG(IOWR)	REG setup time for IOWR	5		ns
thREG(IOWR)	REG hold time from IOWR	0		ns

5.2.5. True-IDE mode I/O access read and write AC characteristics

For the definitions of parameters, please refer to CompactFlash Specification.

Symbol	Parameter	Min.	Max.	Unit
tsuA	Address setup time for IORD/IOWR	70		ns
thA	Address hold time from IORD/IOWR	20		ns
tsuCE	CE setup time before IORD/IOWR	5		ns
thCE	CE hold time following IORD/IOWR	20		ns
tdfIOIS16(ADR)	IOIS16 delay falling from address		35	ns
tdrIOIS16(ADR)	IOIS16 delay rising from address		35	ns
tw	IORD/IOWR pulse width	165		ns
td	Data delay after IORD		100	ns
thD(IORD)	Data hold time following IORD	0		ns
tsuD(IOWR)	Data setup time for IOWR	60		ns
thD(IOWR)	Data hold time following IOWR	30		ns

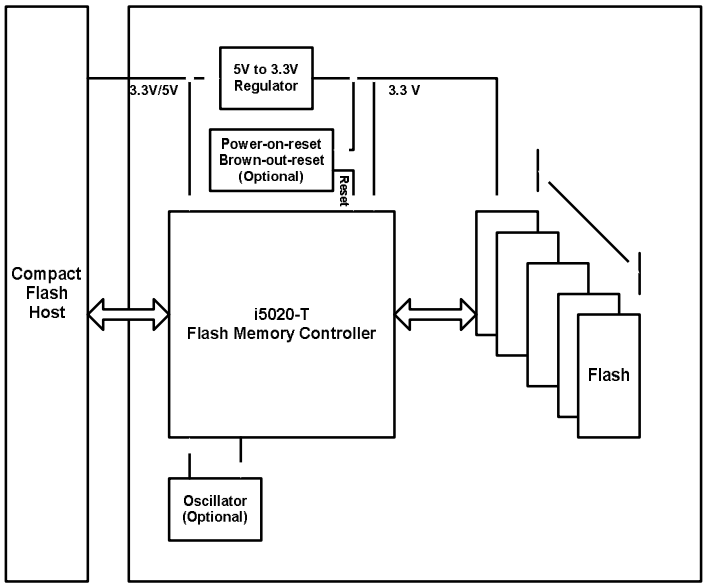
5.2.6. Read/write timing for Samsung / Toshiba type flash

For the definition of parameters, please refer to Samsung/Toshiba flash datasheet.

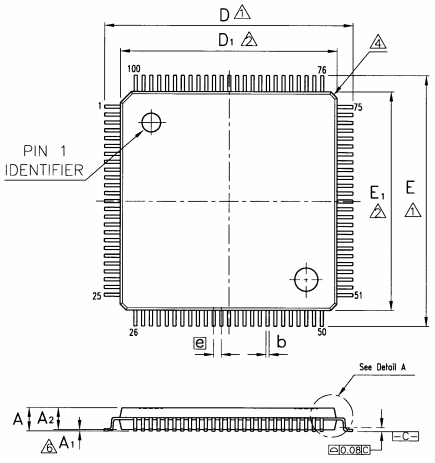
Symbol	Parameter	Min.	Max.	Unit
tCLS	FCLE setup time	0		ns
tCLH	FCLE hold time	10		ns
tCS	FCE# setup time	0		ns
tCH	FCE# hold time	10		ns
tCEH	FCE# high hold time	100		ns
tWP	FWE# pulse width	25		ns
tALS	FALE setup time	0		ns
tALH	FALE hold time	10		ns
tDS	Data Setup time	20		ns
tDH	Data hold time	10		ns
tWH	FWE# high hold time	15		ns
tWW	FWP high to FWE# low	100		ns
tRR	Ready-to-FRE# Falling edge	20		ns
tRP	FRE# pulse width	35		ns
tREH	FRE# high hold time	15		ns
tREA	FRE# access time		35	ns
tWC	Write cycle time	50		ns
tRC	Read cycle time	50		ns
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**

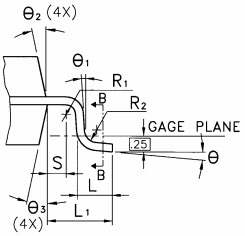
tRHW	FRE# high to FWE# low	0		ns
tWHC	FWE# high to FCE# low	30		ns
tWHR	FWE# high to FRE# low	30		ns
tAR1	FALE low to FRE# low (ID read)	100		ns
tCR	FCE# low to FRE# low (ID read)	100		ns
tAR2	FALE low to FRE# low (read cycle)	50		ns

6. Application example

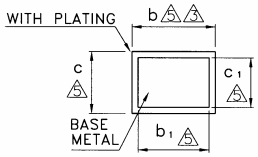


7. Package outline and dimension





DETAIL A



SECTION B–B

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.17	0.22	0.27	0.007	0.009	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	—	0.16	0.004	—	0.630
D	16.00 BSC			0.630 BSC		
D1	14.00 BSC			0.551 BSC		
E	16.00 BSC			0.630 BSC		
E1	14.00 BSC			0.551 BSC		
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°

NOTE :

1. TO BE DETERMINED AT SEATING PLANE -C- .
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS-026 , BED.

iCreate Technologies Corporation
No. 6, Technology Rd. V, Science-Based Industrial Park,
Hsinchu, Taiwan 30077, R.O.C.
Tel: +886-3-579-0000 Fax: +886-3-579-0077